REMARKS/ARGUMENTS

Claims 1-31 were examined.

Allowed/Allowable Claims:

Claims 21-31 were allowed. Claim 26 has been amended to correct an informality.

Claims 2-12 and 15-20 were objected to as being dependent upon a rejected base claim, but were considered allowable if rewritten in independent form including base and intervening claim limitations. Claims 2 -12 and 15 – 20 have been amended to rewrite them to include such limitations.

Rejected Claims:

Claims 1, 13, 14 were rejected under 35 U.S.C. 102(e) as being anticipated by Hochschild (US Pub. 2004/0160348).

The instant application has an effective filing date of 04/15/2003 which is prior to the 06/03/2003 filing date of Hochschild Application No. 10/453,426. Thus, in response to establish a prima facie 102(e) rejection, only the disclosure of Hochschild provisional Application No. 60/447,160 filed 2/13/2003 is relevant.

Hochschild '160 (copy attached) discloses an adaptive quantization system which dynamically sets magnitudes of a given number quantization levels based on input signal magnitude. Quantizer gain is constant, independent of L for output levels {-L, 0, +L}. DAC errors between different values of L appear as gain errors, but don't mix out-of-band quantization noise back in-band. The control block monitors the input signal and increases L as needed to avoid overload for large input signals.

Hochschild '160, inter alia, does not anticipate "a compensation system programmed to mitigate errors associated with a conversion system ... [including] a digital error model programmed to provide an emulated error signal ... [and] having parameters adaptively adjusted ... to emulate error characteristics associated with ... the conversion system."

Thus, the prima facie rejection under 102 (e) of Claims 1, 13 and 14, is rebutted and should be withdrawn. (Applicant reserves the right to swear back of Hochschild, as applicable and if appropriate.)

Accordingly, request is made for reexamination of the application and allowance of the claims, as amended.

Respectfully submitted,

/Warren L. Franz/

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02/14/03 60447160 02/13/03 PROV

02/13/03 JJ1130 U.S. PTO

PROVISIONAL APPLICATION COVER SHEET

JC1046 U.S. PTO 60/447160 02/13/03

This is a request for filing a PROVISIONAL APPLICATION under 37 CFR 1.53 (c).

BOX PROVISIONAL APPLICATION
Commissioner for Patents
Washington, D.C. 20231

Docket Number: TI-35201P (UNITI-165Xq800)	Type a Plus sign (+) inside this box →	+

INVENTOR(s)/APPLICANT(s)

LAST NAME	FIRST NAME	MIDDLE INITIAL	RESIDENCE (CITY AND EITHER STATE OR FOREIGN COUNTRY)
Hochchild	James	R.	2617 Mariposa Circle, Plano, Texas, 75075

[ ] Additional Inventors are being named on Page 2 attached.

TITLE OF THE INVENTION (280 characters max)

VARIABLE, ADAPTIVE QUANTIZATION IN SIGMA-DELTA MODULATORS

CORRESPONDENCE ADDRESS

[X] Customer Number 23494

which is associated with:
W. Daniel Swayze, Jr. Esq.
Texas Instruments Incorporated
P.O. Box 655474, M/S 3999
Dallas, TX 75265
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ENCLOSED APPLICATION PARTS *(CHECK ALL THAT APPLY)*

[X] Specification incl. Figs. Number of pages [10]

[ ] Drawing(s) Number of sheets [ ]

[ ] Small Entity status is entitled to be, and hereby is, asserted for this application.

[ ] Other (specify)

METHOD OF PAYMENT *(CHECK ONE)*

[X] A check in the amount of $160.00 is enclosed to cover the Provisional Filing Fee

[ ] The Commissioner is hereby authorized to charge filing fees and credit Deposit Account Number 23-0804

Please recognize the following attorneys with powers in this application.

Stanley M. Schurgin, Reg. No. 20,979
Charles L. Gagnebin III, Reg. No. 25,467
Victor B. Lebovici, Reg. No. 30,864
Beverly E. Hjorth, Reg. No. 32,033
W. Daniel Swayze, Jr. Reg. No. 34,478
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Respectfully submitted,

SIGNATURE James F. Thompson DATE Feb. 13, 2003

TYPED or PRINTED NAME: James F. Thompson REGISTRATION NO. 36,699

PROVISIONAL APPLICATION FILING ONLY

Express Mail No: EV044744525US
JFT/raw 286532-1

Variable, Adaptive Quantization in ΣΔ Modulators

It is well known that a 2 or 3-level DAC function can be easily made very linear, which is why it is often chosen for ΣΔ converters. Larger numbers of levels usually requires some sort of trim calibration or dynamic element matching techniques to improve the DAC linearity. However, it is possible to adapt the quantizer levels to the input signal amplitude such that at any given time the quantizer produces only 2 or 3 levels, but the magnitude of those levels is controlled by monitoring the input signal. The following figure #1 shows a ΣΔ DAC with variable, adaptive quantization.

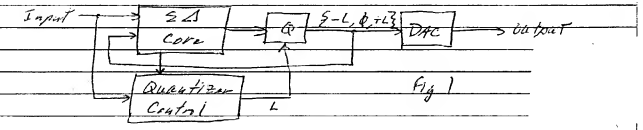


Fig 1

The following figure #2 shows the transfer function(s) of a variable quantizer with output levels {-L, 0, +L} where L ∈ {1, 2, 3, 4}. Note that the quantizer gain is constant, independent of L, which is important for the stability of the system. Provided that the value of L switches infrequently, DAC errors between different values of L appear as gain errors, but don't mix out-of-band quantization noise back in-band, which may be acceptable in some applications such as voice and audio. Figure 3 shows SNR vs Input level for a 4th order ΣΔ DAC similar to Figure 1, with L = 1, 2, 3 and 4.

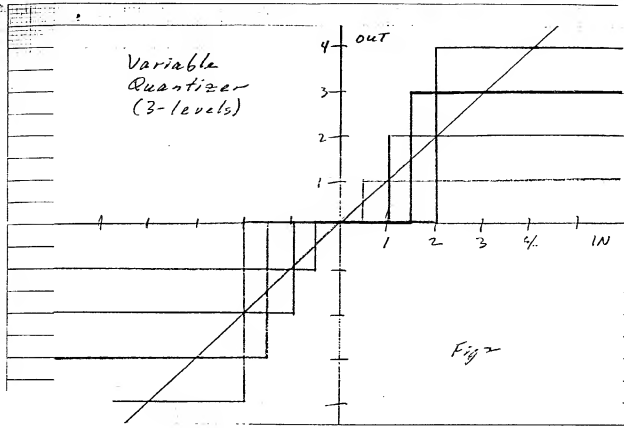


Fig 2

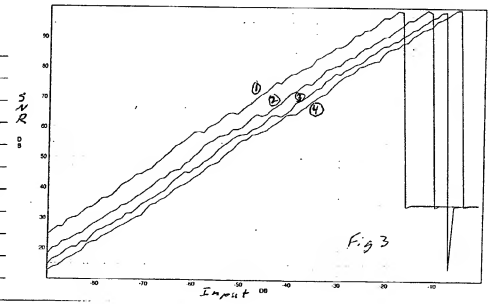
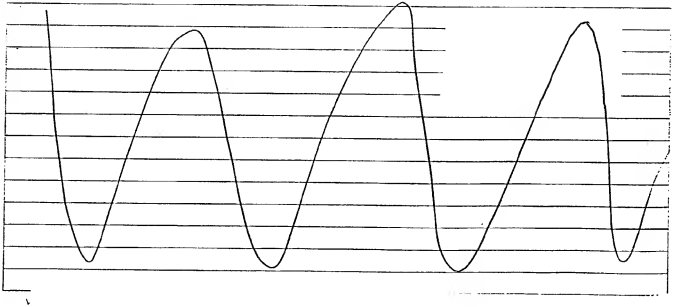


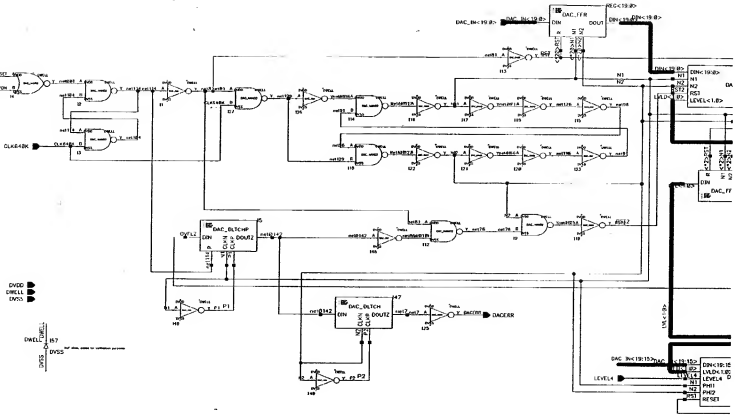
Fig 3

Note that while the SNR is highest for L=1, this level cannot handle signals as large as those for L>1. So, as the input amplitude increases, the value of L must also increase to avoid overload. The Quantizer Control block monitors the input signal and increases L as needed to avoid overload for large input signals. As the input amplitude decreases, the value of L may be allowed to slowly decrease. Decreasing L too rapidly may cause the ΣΔ modulator to ~~become~~ become unstable (which is not a problem for increasing L). Also, a gradual decrease in L reduces the amount of switching of L. Provided that the interval between decreases of L is on the order of milliseconds or perhaps tens of milliseconds, the any audible artifact should be minimal. This system may be useful for many different types of DACs, including those which vary the width of the output pulses to achieve different values of L. Also, the idea may be useful for various types of ADCs.



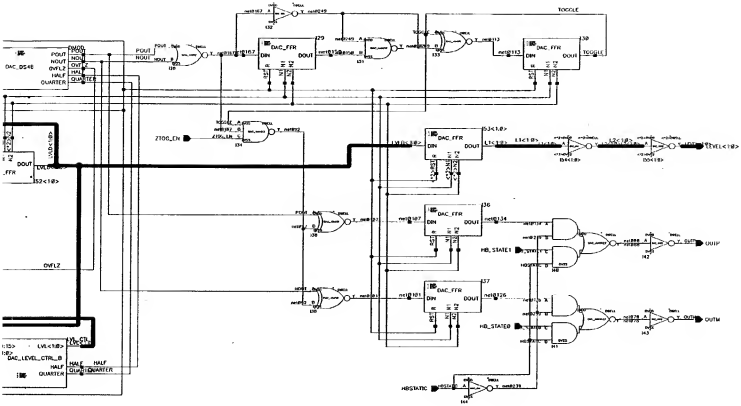
When the quantizer level L is decreased, it is possible for the modulator to become temporarily unstable, even if the input signal level is at or below the maximum signal level which can be reliably processed by the modulator, given the new quantizer level. This is because the previously higher quantizer level may perturb the modulator such that the internal integrator levels are higher than those which would normally be seen given the new lower quantizer level. Also, the "momentum" of the modulator's integrators may be such that the lower level of feedback due to the new lower quantizer level is insufficient to prevent overflow. To prevent this unstable condition, the level of the modulator's integrators may be monitored by the quantizer control block, and based on this information the controller may decide to defer the quantizer level reduction until a later time or to revert to a higher quantizer level if the level was reduced and overflow is imminent.

This description should be accompanied by a modification to the simple block diagram to show a signal representing the state of the modulator's integrators connecting from the sigma-delta core block to the quantizer control block.



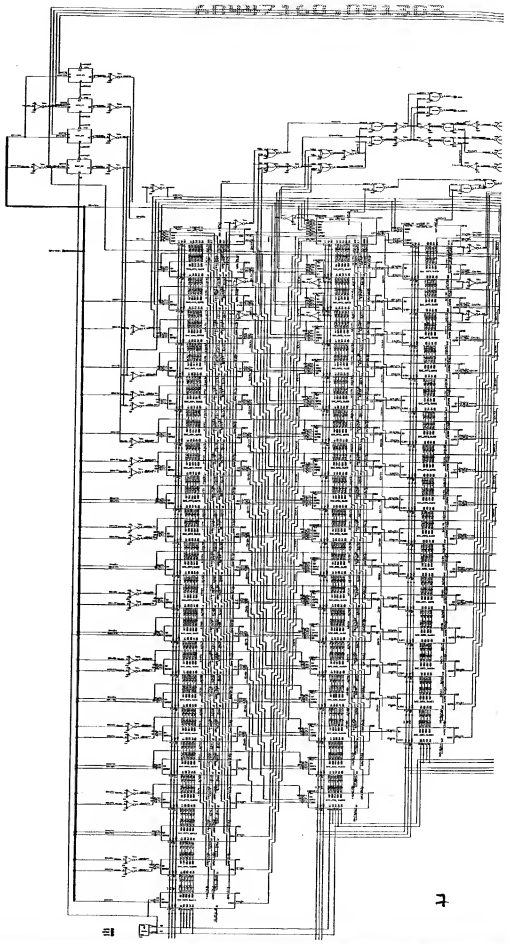
Σ-Δ modulator

1 of 2



Σ-Δ modulators

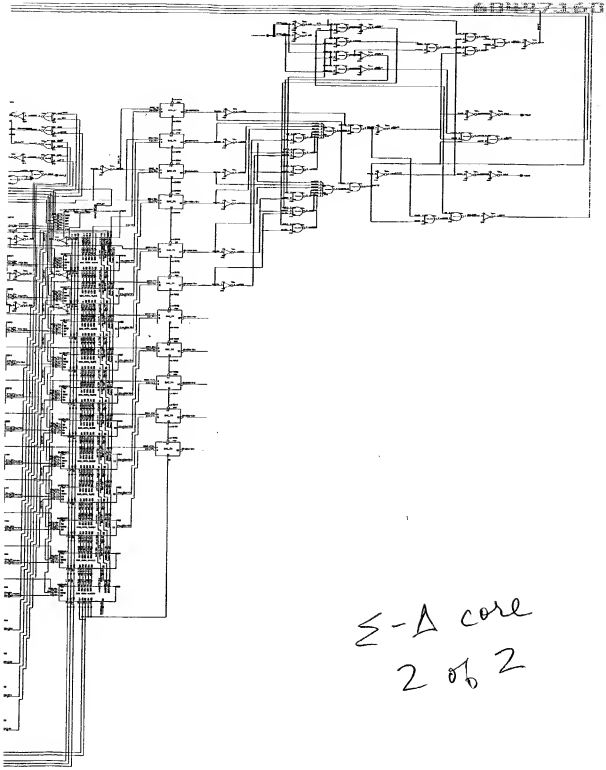
2 of 2



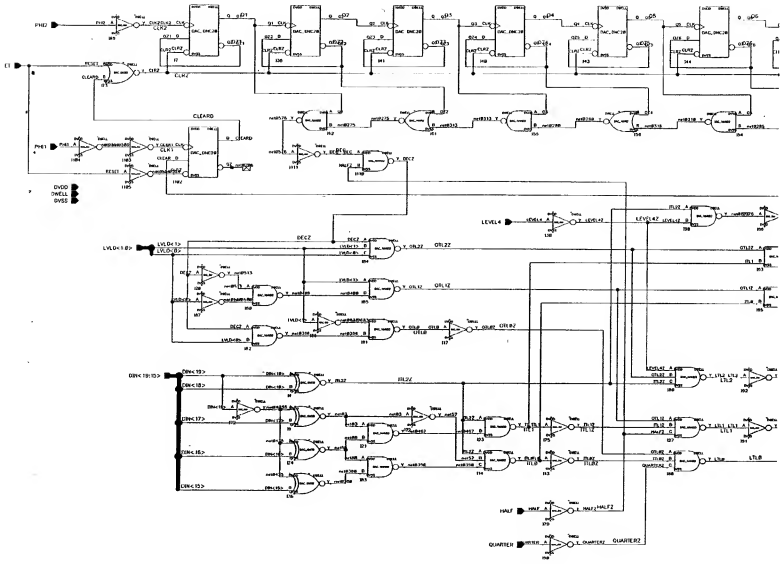
Σ-Δ Core

(DAC-D45B)

1 of 2

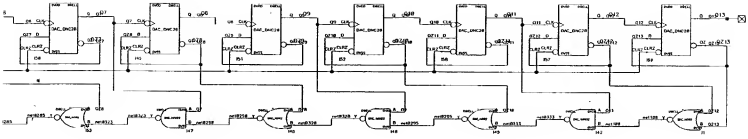


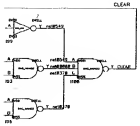
Σ-Δ core
2 of 2

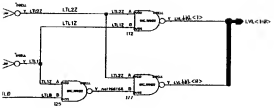


DAC LEVEL CTRL

1 of 2







DAC Level Ctrl.
2 of 2